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# "High Temperature Rectifiers and MOS Devices in 6H-Silicon Carbide"

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**13. ABSTRACT** *(Maximum 200 words)*

A major emphasis in the aerospace industry has been to increase the performance and efficiency of aircraft engines (including helicopters). Most of the improvements require the engine to run hotter, be more compact and more precisely controlled. All of these requirements increase the temperature of an increasing number of electronic components on the engine. This contract involved the development of two types of solid state devices for use in various engine applications using silicon carbide which is the premiere semiconductor material for high temperature (and other) applications. One device is a high voltage, low current rectifier which can operate to at least 350°C for use in an igniter circuit. The developments required involved decreasing the doping level of the background layer in epitaxial growth, improving the passivation and packaging to withstand the high voltage and high temperature. The other is a 350°C small signal MOSFET which can be used as an amplifier for a variety of sensors. For this portion of the research, the major focus was on characterization of the thermal oxide and the oxide interface through fabrication and characterization of MOS capacitors and various MOSFET designs.

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## Table of Contents

## I. Statement of the Problem Studied

A major emphasis in the aerospace industry has been to increase the performance and efficiency of aircraft engines (including helicopters). Most of the improvements require the engine to run hotter, be more compact and more precisely controlled. All of these requirements increase the temperature of an increasing number of electronic components on the engine. This contract involved the development of two types of solid state devices for use in various engine applications using silicon carbide which is the premiere semiconductor material for high temperature (and other) applications. One device is a high voltage, low current rectifier which can operate to at least 350°C for use in an igniter circuit. The developments required involved decreasing the doping level of the background layer in epitaxial growth, improving the passivation and packaging to withstand the high voltage and high temperature. The other is a 350°C small signal MOSFET which can be used as an amplifier for a variety of sensors. For this portion of the research, the major focus was on characterization of the thermal oxide and the oxide interface through fabrication and characterization of MOS capacitors and various MOSFET designs.

## II. Summary

### A. Rectifiers

High voltage, glass packaged rectifiers were developed from 6H-SiC during this research contract. Epitaxial layers of $n^+$-$p^-$-$p^+$ were grown on n-type SiC substrates with a resistivity of 0.02-0.04 Ω-cm. The background doped layer, where depletion in reverse bias is predominant (the $p^-$ layer), was doped at ~1-1.5 x $10^{16}$ $cm^{-3}$ to achieve a high reverse bias breakdown voltage (≥ 1000 V). To obtain 100 mA at a forward voltage of ~3 V, a round mesa junction was formed with an area of 1.5 x $10^{-3}$ $cm^2$ centered on a square chip with dimensions of 480 x 480 μm. Other device fabrication steps included thermal passivation of the mesa junction, ohmic contacts to the top $p^+$ layer and n-type substrate and overlay metals to each for bonding during the packaging process. The rectifier die were packaged in an axial-lead, glass encapsulated configuration. Electrical characterization of these devices was performed via current-voltage and capacitance-voltage measurements. Room temperature reverse voltages as high as ~1375 V were achieved. Current-voltage

measurements showed that a rectifier at a reverse bias of ~1000 V exhibited essentially no reverse current on a 20 μA/division scale at room temperature. When this same device was heated to 350°C, the reverse leakage current at -1000 V remained very low, ~1 μA.

### B. MOS Devices

Several methods have been used during the course of this research to reduce the suspected detrimental effects of Al on the MOS characteristics of 6H-SiC. It was proposed for this contract that the Al dopant present in p-type SiC caused a high interface state density at the SiC / $SiO_2$ interface. Therefore, n-type wafers were grown for MOS capacitors (without Al doping) to further characterize 6H-SiC MOS structures. These capacitors showed very good electrical characteristics, confirming that the presence of Al is the cause of the poor characteristics of p-type SiC.

The first attempts at fabricating p-channel MOSFETs were undertaken. The intent was to show that the improved MOS characteristics of the n-type material could allow p-channel MOSFETs to have as good or better characteristics than n-channel MOSFETs. The initial devices were very poor because of the high Al concentration in the oxide over the source and drain, where the gate overlapped. A thin intrinsic layer of SiC, which was subsequently consumed by oxidation, was utilized in the second batch so that the Al would not be incorporated into the oxide. While very good gate oxides were obtained for these devices, the transfer characteristics were poor and indicated that not all of the thin intrinsic layer had been consumed during oxidation.

Additionally, this same method of negating the effects of Al was investigated on n-channel planar MOSFETs. This again involved growing a thin layer of undoped SiC on top of the structures prior to oxidation which would be consumed during the oxide growth instead of the Al-doped material. This method appeared to work well for the n-channel MOSFETs, showing significantly improved transfer characteristics.

## III. Background

### A. Rectifiers

In order to increase the thrust to weight ratio and efficiency of jet engines, their is a strong need to have a high temperature igniter circuit. This includes engines used on military helicopters. This circuit employs the use of blocking diodes which need to operate at elevated temperatures (>250°C). Silicon carbide diodes (which have been demonstrated to operate reliably up to 350°C) should be ideal for this application. The voltage which must be blocked is 4500 V. At present, twenty silicon rectifiers which are derated from 600 V at RT to 200 V at 260°C are "hand-picked" and used in a stack to block this voltage. However, this stack cannot be used at temperatures >260°C and the leakage current is ~100 μA at 260°C. Silicon carbide rectifiers do not have to be voltage derated to at least 350°C and have leakage currents <1 μA at this temperature. High voltage diodes developed from SiC would reduce the number of devices required without derating of the device. Prior to this research only low to medium voltage (50-500 V) diodes had been developed in SiC. The first objective of this research was to fabricate SiC chips with a reverse breakdown voltage ($V_{br}$) of >1000 V and forward current rating of 100 mA.

Packages for these chips require high temperature and harsh environment operation. An axial lead, glass imploded package was the package chosen for this research. Unlike previous packages developed for SiC rectifiers, these devices must insulate against high potentials (>1000 V) in a relatively small distance. This requires a voidless bond between chip passivation and the glass package itself. Development of this type of encapsulant was the second objective of this research. Results of electrical characterization of these packaged rectifiers is given.

### B. MOS Devices

Fabrication of MOS structures at Cree on 6H-SiC p-type layers had shown that dry oxides grown on the Si-face generally have high fixed oxide charge levels ($Q_{eff}$), in the mid $10^{12}$ $cm^{-2}$ range. Current-voltage measurements also showed that these oxides had very high leakage currents after annealing in Ar at high temperature (900-1000°C); these leakage currents were greatly reduced by annealing in Ar/4%$H_2$

instead of Ar. The dry oxide having the lowest value of $Q_{eff}$ = 4-5x$10^{12}$ $cm^{-2}$ was grown at 1300°C.

The MOS C-V measurements of Si-face samples after wet oxidation were much more encouraging. The C-V curve shown in Fig. 1 shows the typical characteristics of the samples that were measured by Hg probe. This particular oxide was grown at 1100°C in wet $O_2$ for 360 minutes, resulting in an oxide thickness of 49.5 nm. The flatband voltage ($V_{fb}$) and threshold voltage ($V_{th}$) were measured to be -5.4 V and +1.5 V, respectively, corresponding to a fixed oxide charge ($Q_{eff}$) of 1.2x$10^{12}$ $cm^{-2}$. This curve was virtually identical in either sweep direction.

Another positive trend that was observed for the wet oxides grown on the Si-face was that the higher the oxidation temperature, the lower the $Q_{eff}$ after subsequent contact annealing at 925°C. The $V_{fb}$ and $V_{th}$ of a wet oxide grown at 1100°C and annealed in Ar/4%$H_2$ was -16.3 V and -9.7 V while the $V_{fb}$ and $V_{th}$ of a wet oxide grown at 1300°C and annealed was -10.0 V and +1.3 V. The average measured fixed oxide charges at 1100°C, 1200°C, and 1300°C were 5.5x$10^{12}$ $cm^{-2}$, 3.8x$10^{12}$ $cm^{-2}$, and 2.6x$10^{12}$ $cm^{-2}$, respectively.

As indicated above, the effects of oxidation conditions and subsequent annealing on the C-V characteristics of 6H-SiC MOS structures has been conducted at Cree. While much improvement has been achieved in reducing the fixed oxide charge by optimizing the oxide processing, the C-V characteristics of MOS structures on Al-doped p-type material still show relatively high $Q_{eff}$ in the 1-3x$10^{12}$ $cm^{-3}$. Additionally, n-channel MOSFETs fabricated in p-type 6H-SiC have shown high threshold voltages, low channel mobilities, and large variation of output with temperature. Previous research on n-type β-SiC has shown much lower $Q_{eff}$[1] in the range of 2-4x$10^{11}$ $cm^{-3}$. Although there has been very little MOS research performed on n-type 6H-SiC, it was to logical to assume that the $Q_{eff}$ values would also be in this low $10^{11}$ range. The reason for the large difference in oxide charge between n-type and p-type SiC was proposed to be to the very high Al concentration present in the p-type films.

The activation energy for Al in 6H-SiC is in the range of 0.20 eV, and the typical level of donor compensation is about $N_D$ = 5-10x$10^{15}$, which means that a p-type 6H-SiC film with a hole concentration in the range of 1x$10^{16}$ $cm^{-3}$ at room

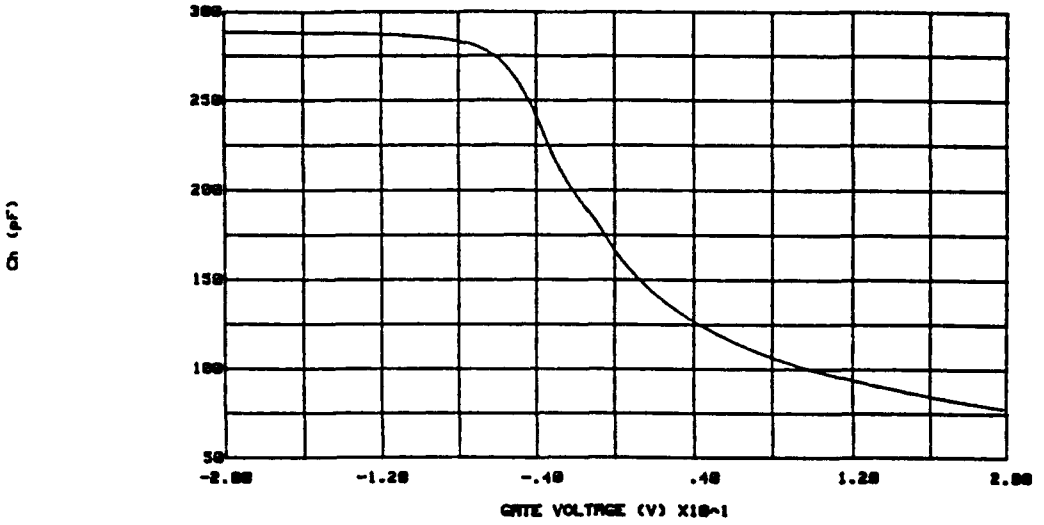



Figure 1. Capacitance-voltage curve measured on a double column Hg probe of an oxide layer grown in wet $O_2$ at 1100°C for 360 mins. on the Si-face of 6H-SiC. The starting p-type layer was doped $8.5x10^{16}$ $cm^{-3}$ and the oxide thickness was 49.5 nm.

temperature has an Al atomic concentration in the range of $0.7\text{-}1x10^{17}$ $cm^{-3}$. This high level of $N_A$ could greatly increase the interface state density, because it would alter the structure of the $SiO_2$ and the $SiO_2$/SiC interface. Lastly, a high concentration of Al in the SiC would certainly decrease the channel mobility of the charge carriers in an inversion layer simply by impurity scattering. Therefore, it was proposed that p-channel MOSFETs could have significantly better transfer characteristics than n-channel MOSFETs. Although the hole mobilities in p-type SiC are quite low (~20-80 $V/cm^2$-sec), the improved MOS characteristics of the n-type SiC could outweigh this disadvantage. All of the n–channel MOSFETs fabricated in 6H-SiC prior to this contract were limited by their high interface charge densities and low channel mobilities.

Cree has already shown that much improved room temperature characteristics had been achieved for planar n-channel MOSFETs fabricated with channel layers doped on the order of $p = 2\text{-}4x10^{15}$ $cm^{-3}$. As the Al concentration was decreased, the transfer characteristics progressively improved. Previous MOSFET structures had p-

type doping in the range of 2-8×$10^{16}$ $cm^{-3}$, which demonstrated very low transconductances and very high room temperature threshold voltages. This further confirms the hypothesis that the Al dopant from the SiC causes interface traps and high positive charge in the oxide.

## IV. Rectifiers

### A. Mask Design

The rectifiers developed in this research are rated at 100 mA at a forward bias of ~3 V at room temperature with a $V_{br}$ of >1000 V at 350°C. To achieve the latter, reverse bias breakdown data from lower voltage diodes previously characterized was extrapolated to higher voltages. The experimental relationship between $V_{br}$ and the minimum depletion width ($W_m$) versus the background doping ($N_B$) for an abrupt junction in 6H-SiC is shown in Figure 2. From this plot, the value of $N_B$ for the lower doped epitaxial layer was targeted for 1-1.5 x $10^{16}$ $cm^{-3}$ with a thickness of 10-15 μm. This layer represents approximately 90% of the total resistance of the final rectifier die and thus is the critical layer in determining the size requirement for the mesa junction.

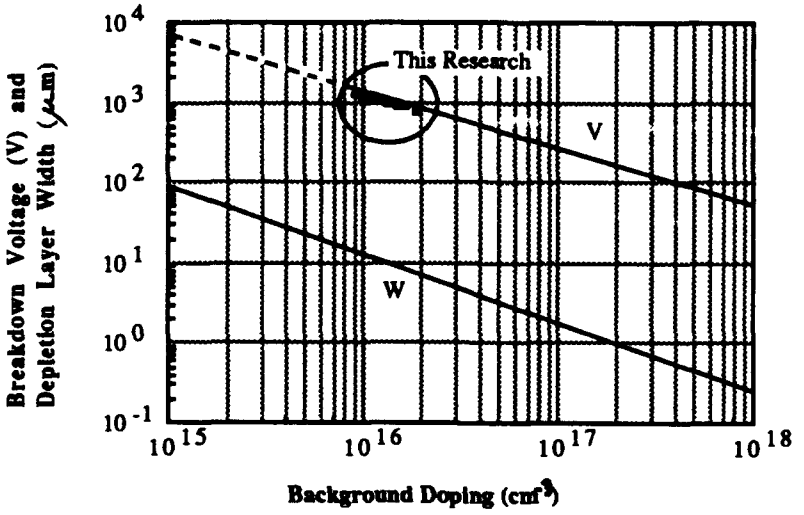



Figure 2. Relationship between the breakdown voltage and minimum depletion width versus the background doping of a 6H-SiC p-n junction diode. Added data points are a result of the present research.

The built-in potential of the 6H-SiC junctions is ~2.6 V. To achieve 100 mA at 3 V, the total resistance of the die can be:

$$(3\text{-}2.6)\ V/0.1\ A = 4\ \Omega$$

The resistivity of p-type 6H-SiC doped to 1-1.5 x $10^{16}$ $cm^{-3}$ is ~5 Ω-cm. With a thickness of 12 μm and resistance of 4 Ω, the area of the mesa junction is given by:

$$A = (5\ \Omega\text{-cm})(12 \times 10^{-4}\ cm)/4\ \Omega = 1.5 \times 10^{-3}\ cm^2$$

The diameter of a circular mesa junction must then be ~430 μm. From this calculation the mask was designed as circular mesa junctions with a diameter of 430 μm centered on a square die with an edge length of ~480 μm. The mask design for the ohmic contact to the top of the mesa is circular with a diameter of 330 μm.

## B. Device Structure

Wafers of $n^+$ 6H-SiC with typical resistivities in the range of 0.02-0.04 ohm-cm were used as substrates. Their thickness was typically 250-275 μm. An epitaxial junction was produced thereon by first growing an $n^+$ layer with a carrier density of ~3 x$10^{18}$ $cm^{-3}$, followed by a $p^-$ layer, and finally a $p^+$ layer. The depletion layer occurred predominantly in the $p^-$ layer and typically had a carrier concentration of 1-1.5 x $10^{16}$ $cm^{-3}$ and was 10-15 μm thick. This resulted in a reverse breakdown voltage in the range of 1000-1500 V. The $p^+$ layer was used to achieve a low contact resistance on the p-side of the junction. The resistivity of this layer was typically 0.1-0.2 ohm-cm with a hole density of 5-15 x $10^{19}$ $cm^{-3}$. The wafer was then ready for device fabrication.

From the calculation above, the required junction area of these rectifiers was 1.5 x $10^{-3}$ $cm^2$. The total chip area (square shape) as well as the $n^+$ side ohmic contact area was 2.3 x $10^{-3}$ $cm^2$ whereas the $p^+$ side contact area was 8.6 x $10^{-4}$ $cm^2$. Etching of the mesa junctions was accomplished utilizing reactive ion etching with $NF_3$ gas. The mask for the etch was Al. The junctions were passivated with 0.5 μm of thermally grown $SiO_2$. Ohmic contact materials for the p-side and n-side were sintered Al and Ni, respectively. An overlay metal system of Ti/Pt/Au was then applied to the ohmic contacts as bond layers for wire bonding or brazing of the chip

in a package. The thickness of these layers was 0.1 μm for both the Ti and Pt followed by 0.5 μm of Au. All metal layers were deposited via d-c magnetron sputtering. Figure 3 schematically shows a cross-section of the completed SiC rectifier chip.

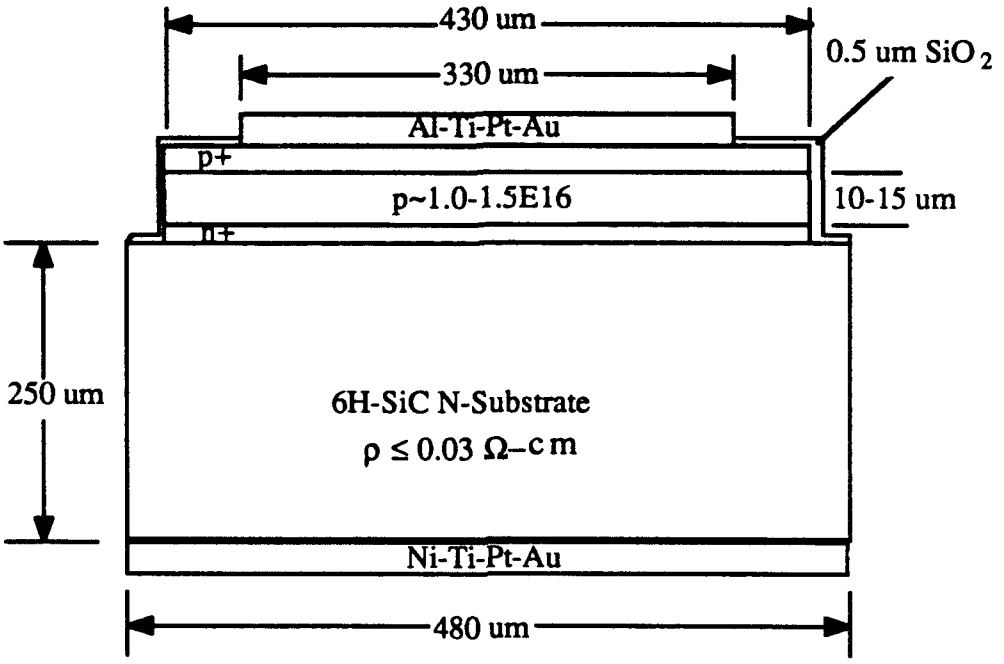



Figure 3. Schematic drawing of the cross-section of a 6H-SiC 100 mA/3 V rectifier chip design to reach a breakdown voltage of >1000 V.

### C. Electrical Characterization of Chips

For these devices, both capacitance-voltage (C-V) for determining the background doping and current-voltage (I-V) measurements were performed. Figure 4 shows the background doping level for a diode with a reverse breakdown voltage ($V_{br}$) of ~1100 V. The layer was depleted to a reverse bias of -20 V for the C-V measurement. As shown in this figure, the background doping level of this junction increased from ~6 x $10^{15}$ $cm^{-3}$ at the junction interface to ~1.1 x $10^{16}$ $cm^{-3}$ after ~1.0 μm depletion. Using the ending (-20 V) carrier concentration value obtained using the C-V measurement and the breakdown voltage measured from I-V, a number of data points have been added to the $V_{br}$ curve in Figure 2. As shown in this figure, the results of the present research closely matches the extrapolated curve (dotted line). The slight difference is probably due to the slight increase in the background doping concentration beyond the ~1 μm depth measured by C-V. A slight increase in $N_B$ would shift the data points to the right, lying more closely to the extrapolated curve.

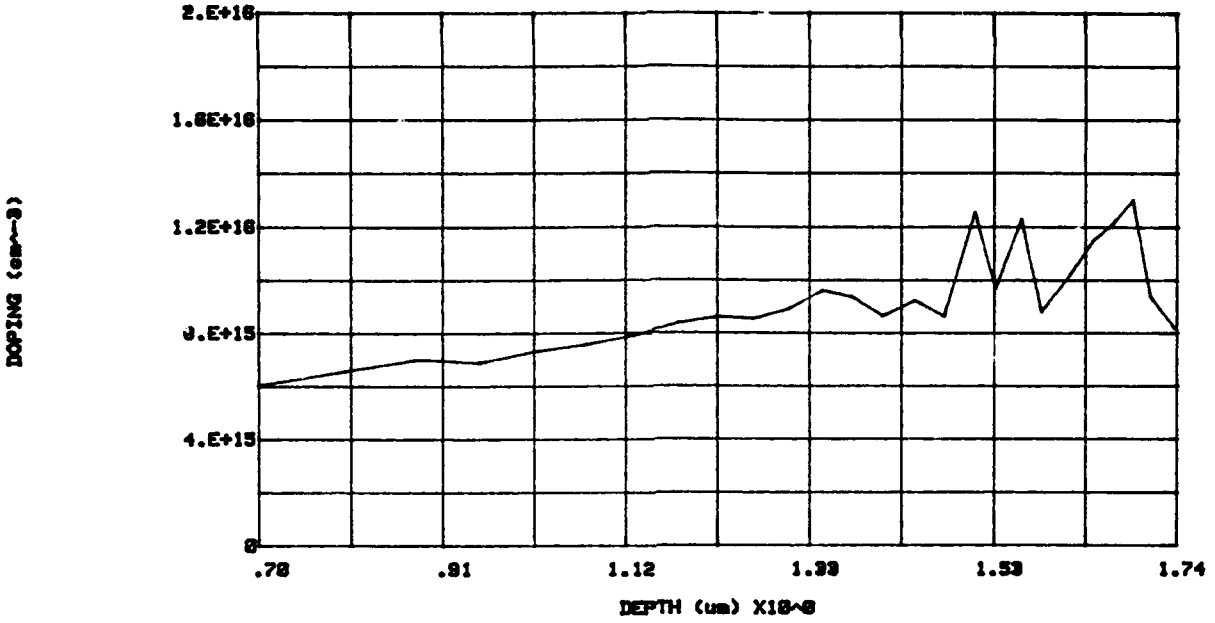


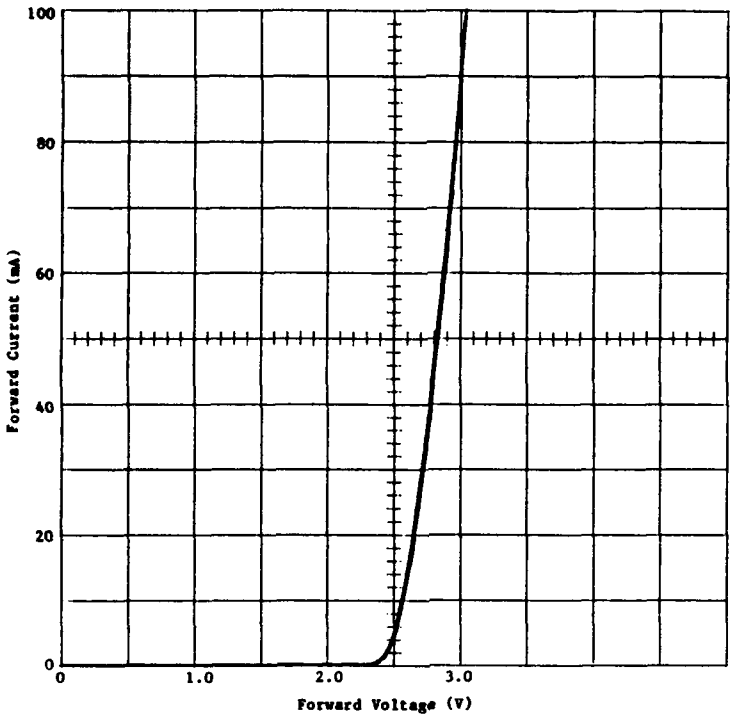

Figure 4. Capacitance-voltage measurement of a 6H-SiC rectifier to -20 V showing the doping profile versus distance in the background doped layer. The device exhibited a reverse breakdown voltage of ~1100V.

Figures 5a and 5b show the room temperature forward and reverse bias I-V characteristics, respectively, of a 6H-SiC rectifier with $V_{br}$ ~ 1100 V. As shown in the forward bias curve, the device turns on ~2.5 V and the current increases rapidly beyond ~2.6 V to 100 mA at ~3 V, the target voltage. In reverse bias, the device exhibits avalanche multiplication breakdown at ~1100 V. The leakage current prior to avalanche is extremely low, ~1 μA.

Figures 6a and 6b show the forward and reverse bias I-V characteristics of a packaged rectifier operating at room temperature and 350°C, respectively. At room temperature, the reverse leakage current at -1000 V is essentially 0 on a 20 μA/division scale. When it is heated to 350°C, the leakage current increases to ~1 μA at -1000 V. As has been determined in previous research, the built-in junction potential and thus the forward bias at the rated current (100 mA) decreases at a rate of 1.5 mV/°C or ~0.5 V from room temperature to 350°C.

Figure 7 shows the I-V characteristic of the highest voltage packaged rectifier achieved in this research. As shown on the 5 μA/division vertical scale, the device exhibited <1 μA leakage at a reverse voltage of ~1375 V. This at the onset of avalanche

(a)

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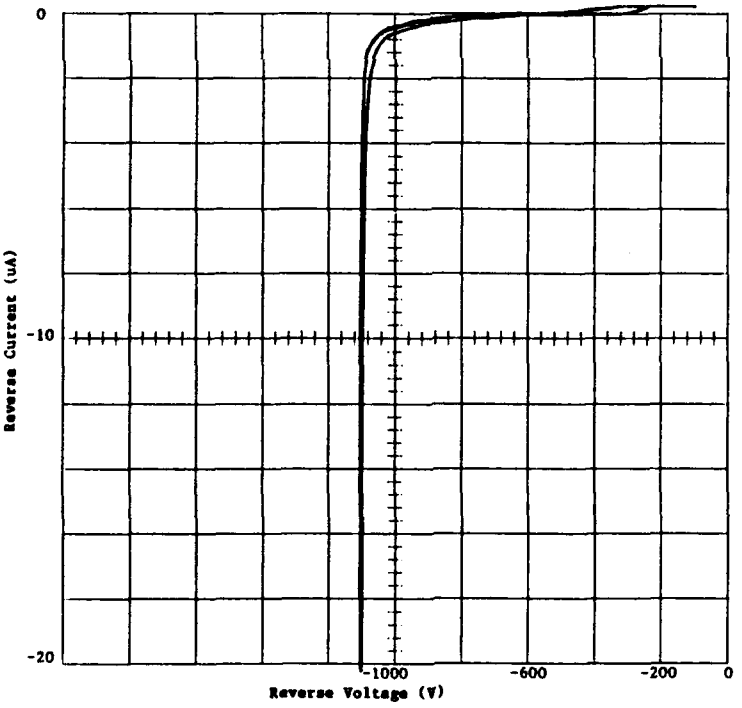
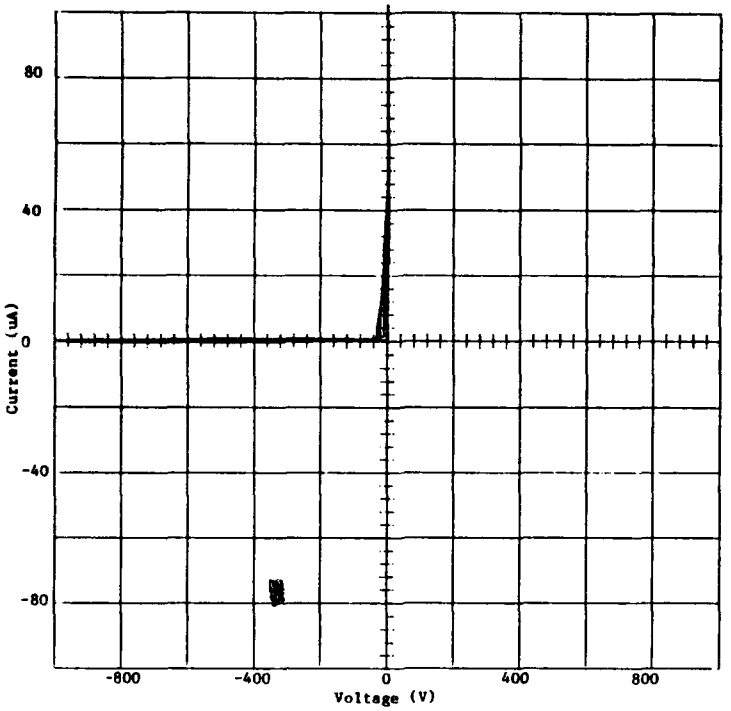



Figure 5. Current-voltage curves of the rectifier characterized in Fig. 4 showing (a) the forward bias characteristics to 100 mA and (b) the reverse bias characteristics to avalanche breakdown at ~1100 V.

(a)

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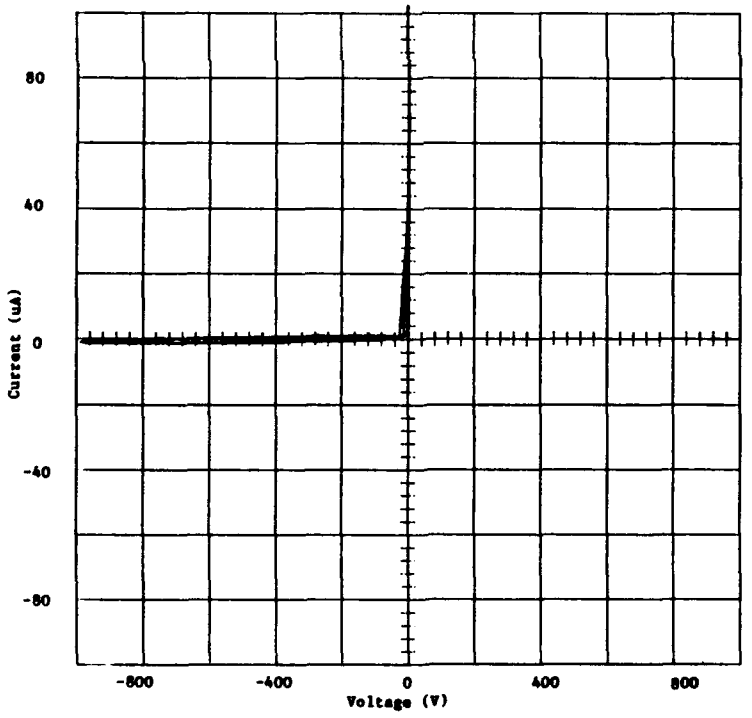


Figure 6. Current-voltage curves of a 6H-SiC rectifier emphasizing the reverse bias characteristics to 1000 V while operating at (a) room temperature and (b) 350°C.

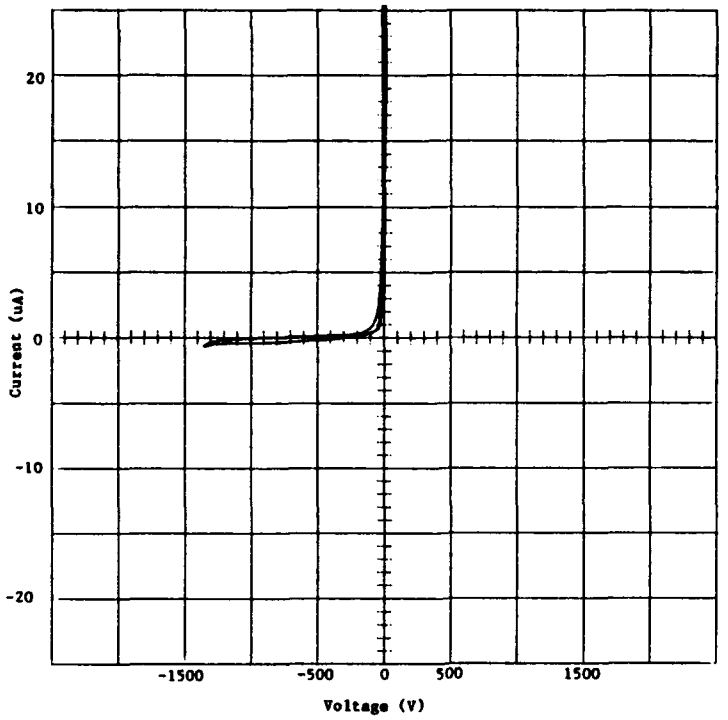


Figure 7. Current-voltage curve of a 6H-SiC rectifier with a reverse bias breakdown at ~1375 V. The device was operating at room temperature during the measurement.

breakdown. At higher levels of reverse current the devices typically failed. Further research is needed to determine and address the failure mechanism.

### D. Packaging

One of the objectives of this contract was to develop a packaging scheme that would result in a voidless, hermetically sealed glass package capable of withstanding voltages of ≥1000 V and operation at 350°C. The former criteria was the first to be tested. Using the packaging scheme developed at Cree for lower to medium voltage devices, internal arcing occurred across the junction at voltages of 950-1000°C. The atmosphere for the glass firing profile was initially pure nitrogen. Using this atmosphere, essentially all parts failed catastrophically at ~1000 V with a short forming across the junction between the passivation layer of the chip and the glass sleeve interface. From these results it was determined that the bond between these two glasses was insufficient. To improve this interface, oxygen was added to the glass firing atmosphere. The first gas mixture attempted utilized a mixture of 99.5% $N_2$ and

0.5% $O_2$. This increased the voltage for catastrophic failure to 1100-1200 V. After observing this improvement, a gas mixture of 95% $N_2$ and 5% $O_2$ was evaluated. This resulted in the highest voltage package that was obtained at the time of the contract end. A voltage of ~1400 V was obtained using this atmosphere. Figure 8 shows the glass firing profile for this packaging scheme.

The composite 100 mA glass encapsulated, axial-leaded rectifier package utilizes a 30 mil diameter molybdenum slug, headed copper leads, Au-Ni braze preforms (82% Au/18% Ni) and glass sleeve (see Figure 9). The leads are first brazed to the slugs at 950°C for 2 min. in $N_2$. The piece parts (leads with slugs, SiC chips and glass sleeve) are loaded into a graphite boat and heated in a vacuum furnace under the conditions described above. This results in a compression bonded, voidless and hermetically sealed package. In order to operate at 350°C in air, the leads are then gold plated in a separate operation.

Some fine tuning is still required for the encapsulation process. To achieve higher voltages and higher reliability, more research in the packaging must be performed.

## V. MOS Capacitors

Wafers for n-type MOS capacitors were grown on both Si-face and C-face to determine the quality of the oxides. The substrates were n-type and were sliced from N-doped 6H-SiC crystals. The wafer surfaces were then lapped, polished and cleaned in preparation for epitaxial growth. Four wafers were polished on the C-face and three were polished on the Si-face. Thin films of n-type 6H-SiC were then grown on the substrates. The doping range used was $n = 1.3\text{-}2.4\times10^{16}$ $cm^{-3}$. This doping level is similar to that used for the p-channel MOSFETs.

These devices were fabricated by growing oxide layers in wet $O_2$. The Si-face oxides were grown at 1100°C for 690 minutes, resulting in an $SiO_2$ thickness of 615 Å, while the C-face wafers were oxidized at 1050°C for 40 minutes resulting in an oxide thickness of about 650 Å. The oxide was then etched off of the back of the wafers with reactive ion etching and 200 nm of Ni was deposited for ohmic contact to the substrates. The molybdenum electrodes, which had an area of $3.38\times10^{-3}$ $cm^{-2}$, were patterned on the topside oxide layers using the lift-off process.

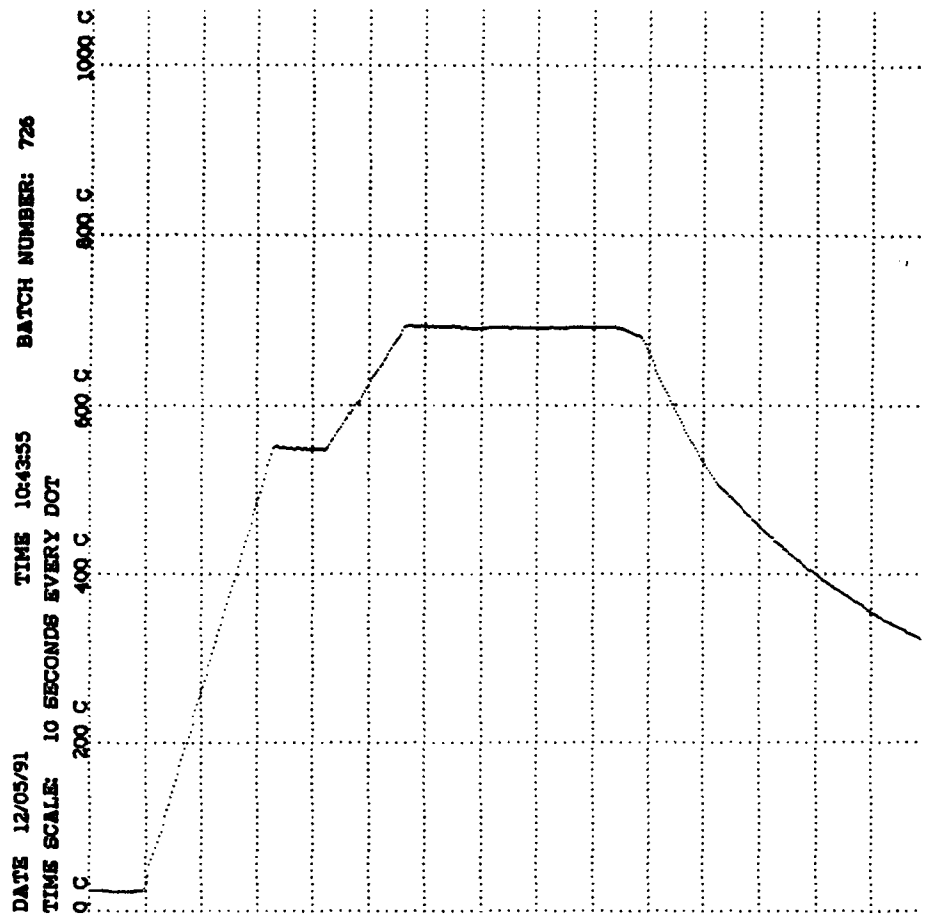


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Figure 8. Glass firing profile developed for the packaging of axial-lead rectifiers which yielded the highest reverse voltage capability.

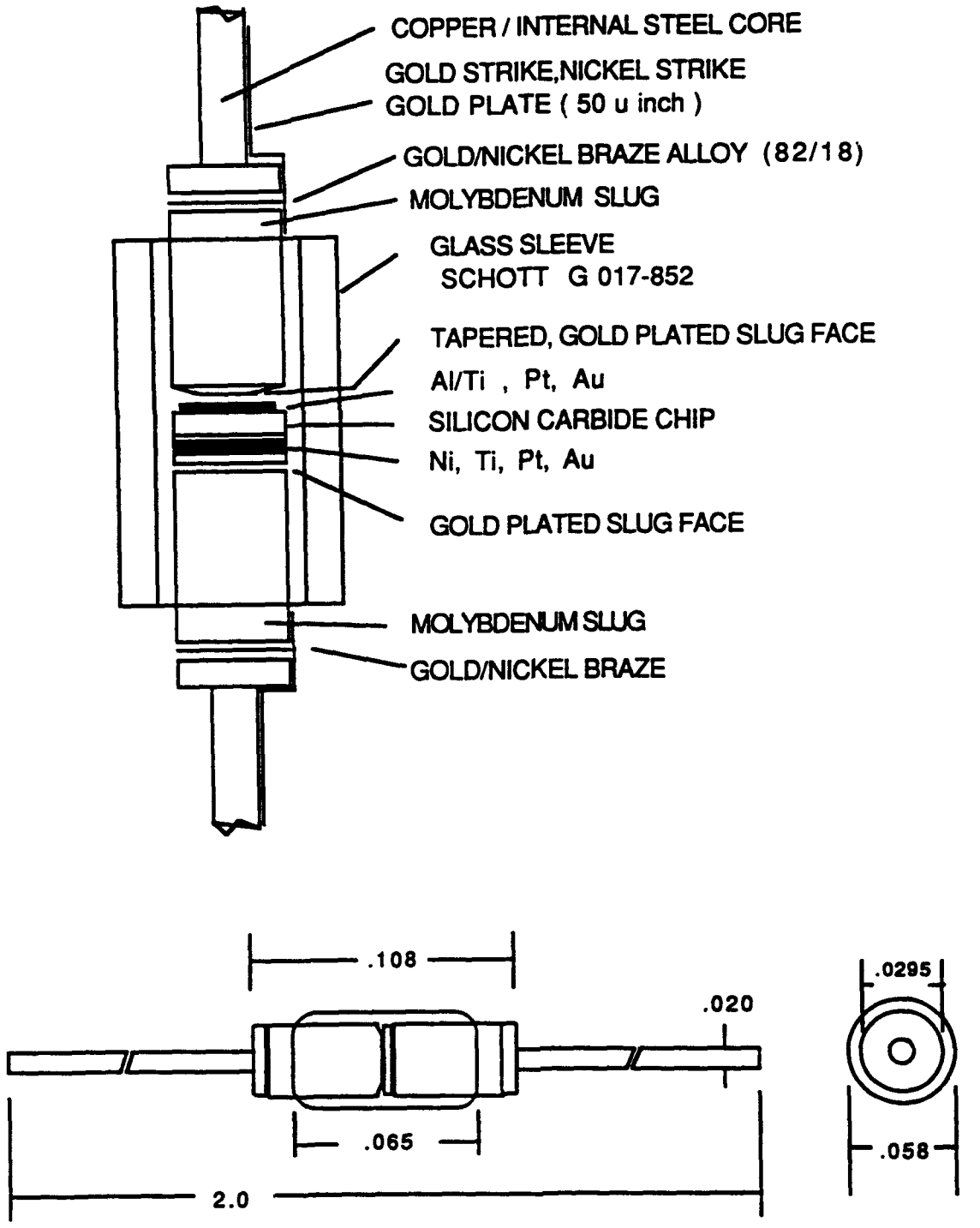



Figure 9. Schematic showing the composite of the 100 mA glass encapsulated, axial-leaded rectifier package developed in this research.

As was expected, the C-V curves of the n-type MOS capacitors had very good characteristics. The MOS curve in Fig. 10 shows very nice characteristics for an oxide grown at 1100°C on the Si-face, with a $C_{min}$ / $C_{max}$ ratio of 0.17. The carrier concentration was previously measured to be n = $2.4 \times 10^{16}$ $cm^{-3}$. The flatband voltage was calculated to be at 0.12 V, and the threshold voltage was calculated to be at -4.7 V. The fixed oxide charge was less than $5 \times 10^{10}$ $cm^{-2}$. These characteristics are far better than the characteristics for the Al-doped p-type 6H-SiC MOS capacitors that were discussed earlier, which were oxidized under the same basic set of conditions. Similar results have been reported by Brown, *et al.*[2], where the oxides grown on n-type material had no detectable oxide space charge ($\leq 5 \times 10^{10}$ $cm^{-2}$), fast interface states ($\leq 5 \times 10^{10}$ $cm^{-2}eV^{-1}$), or slow traps ($\leq 5 \times 10^{10}$ $cm^{-2}$), as shown in Fig. 11. Brown, *et al.* also observed very high interface trap density ($3 \times 10^{12}$ $cm^{-2}eV^{-1}$) for oxides grown on the Al-doped p-type material. Therefore it can be concluded that the very high fixed oxide charge and interface trap density observed for the p-type material is due to the Al dopant.

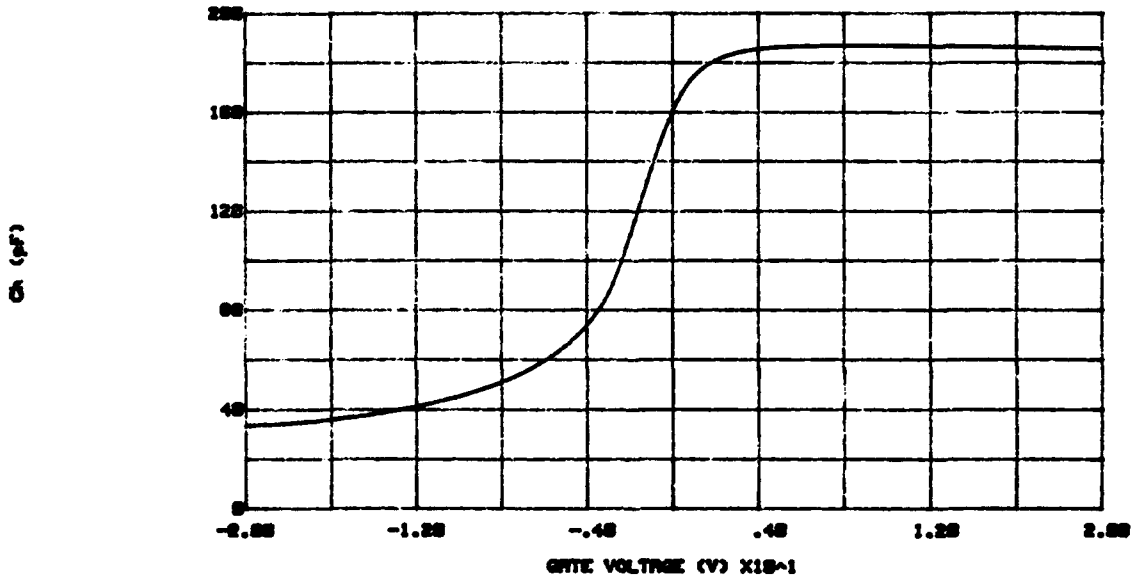



Figure 10. Capacitance-voltage curve measured on a MOS capacitor with an oxide grown in wet $O_2$ at 1100°C for 690 mins. on the Si-face of an n-type epilayer with n=$2.4 \times 10^{16}$ $cm^{-3}$.

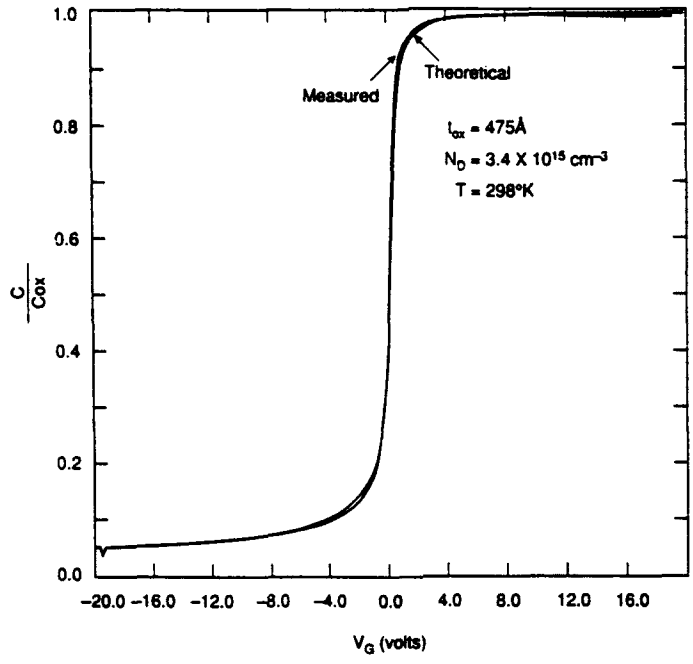



Figure 11. Experimental and theoretical normalized capacitance-voltage curves[2] measured on a MOS capacitor with an oxide grown in wet $O_2$ on the Si-face of a n-type epilayer with $n=3.4x10^{15}$ $cm^{-3}$. The gate electrode was Mo.

The results of the C-face MOS capacitors were not as conclusive. These devices had high oxide leakage currents. This has been an intermittent problem for C-face wafers, although it is uncertain whether the leakage was caused by the fact that the wafers were C-face, or whether the leakage current was due to a processing error. It is suspected that C-face probably does have inferior oxides compared to Si-face wafers, but more experimentation is required.

Wafers with MOS capacitors fabricated on both n-type and p-type 6H-SiC were sent to Dr. Jim McGarrity at Harry Diamond Laboratories so that he may begin experimentation on the radiation hardness of these structures. In addition to the fabricated devices, two bare n-type wafers were also grown and sent to Dr. McGarrity as a part of this contract, so that he may also fabricate some MOS structures for independent verification of these results and for further evaluation of the radiation hardness of SiC MOS structures. Three other wafers were also grown and sent to Harry Diamond Laboratories for use in Hall Effect measurements.

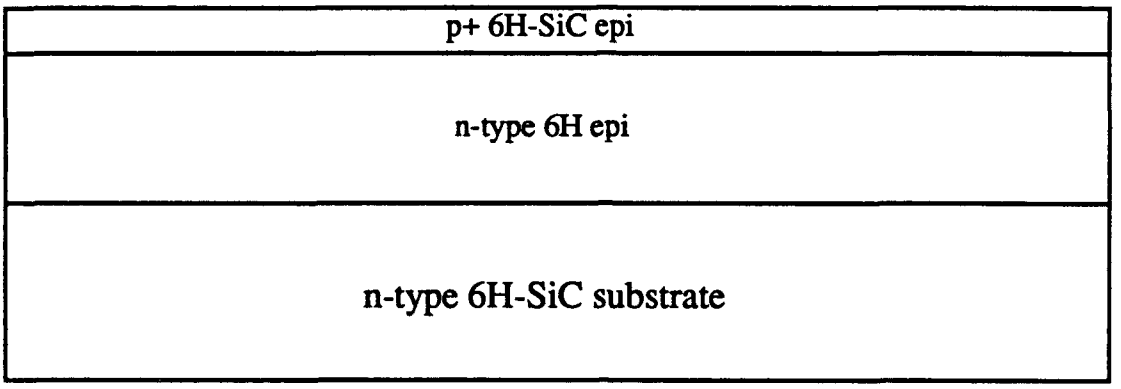
## VI. Planar MOSFETs

### A. p-channel MOSFETs

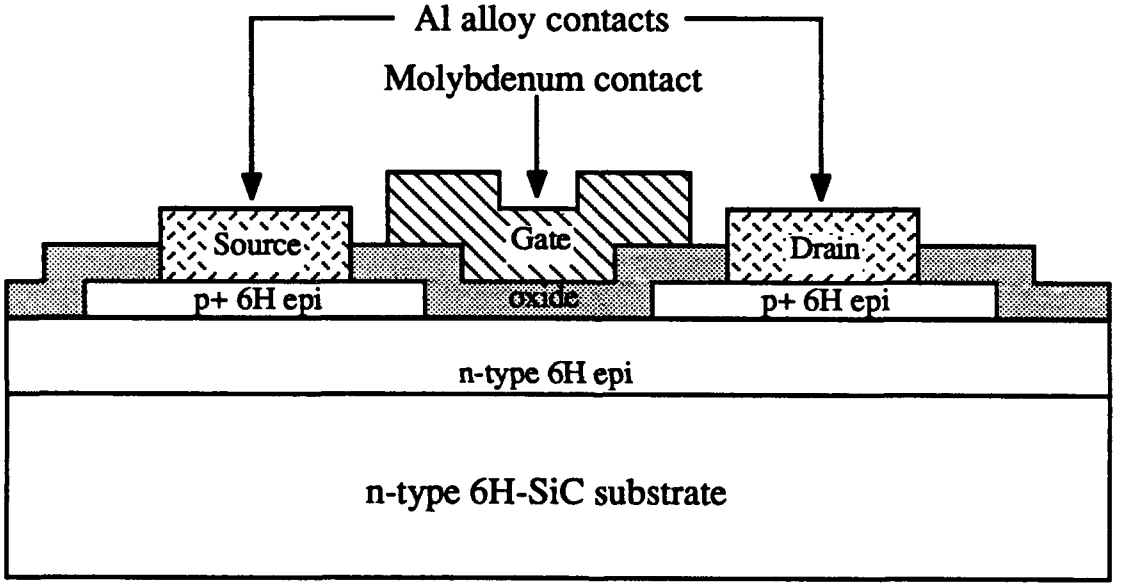
Because of the high interface trap density observed for the oxides grown on p-type SiC, it was proposed that p-channel MOSFETs could have as good, if not better, transfer characteristics than n-channel MOSFETs. Two batches of p-channel MOSFETs were fabricated during this effort. The first batch had the design shown in cross-section in Fig. 12(a) and (b). The $p^+$ source and drain areas were first grown by epitaxy and then patterned into mesas using reactive ion etching in $NF_3$. The reason this process was used instead of ion implantation is that implantation of $Al^+$ into 6H-SiC has not been investigated to the point where it was certain it could be done successfully.

After formation of the $p^+$ source and drain mesas, the oxide layers were grown. Both Si- and C-face wafers were fabricated. The Si-face wafers were oxidized at 1200°C in wet $O_2$ for 33 minutes and the C-face wafers were oxidized in wet $O_2$ at 1100°C for 11 minutes. The resulting oxide thicknesses were about 600 Å. After oxidation, the Al-alloy contacts to the source and drain areas were patterned, and then the molybdenum gate contact was patterned in between the source and drain, overlapping the $p^+$ mesas, as shown in Fig. 12(b). The device layout, shown in Fig. 13, utilized an interdigitated structure with a three-fingered source contact and a two-fingered drain contact.

While the visual characteristics of the first batch of p-channel MOSFETs looked very good, the electrical characteristics of these devices were very poor. All of the devices measured were dominated by very high gate leakage current (>5 mA). Because of this high leakage current, there were no desirable transfer characteristics. It was assumed that the high gate oxide leakage current was caused by the very high Al concentration in the oxide where the gate contact overlapped the $p^+$ source and drain mesas. The atomic Al concentration in these areas could exceed $10^{21}$ $cm^{-3}$, causing a very contaminated, electrically leaky oxide to grow. Therefore the devices are rendered useless, even though the oxide over the n-type material has very good electrical characteristics.




(a)




(b)

Figure 12. Cross-sectional view of (a) the beginning epitaxial structure and (b) the final device structure of the 6H-SiC p-channel MOSFETs.

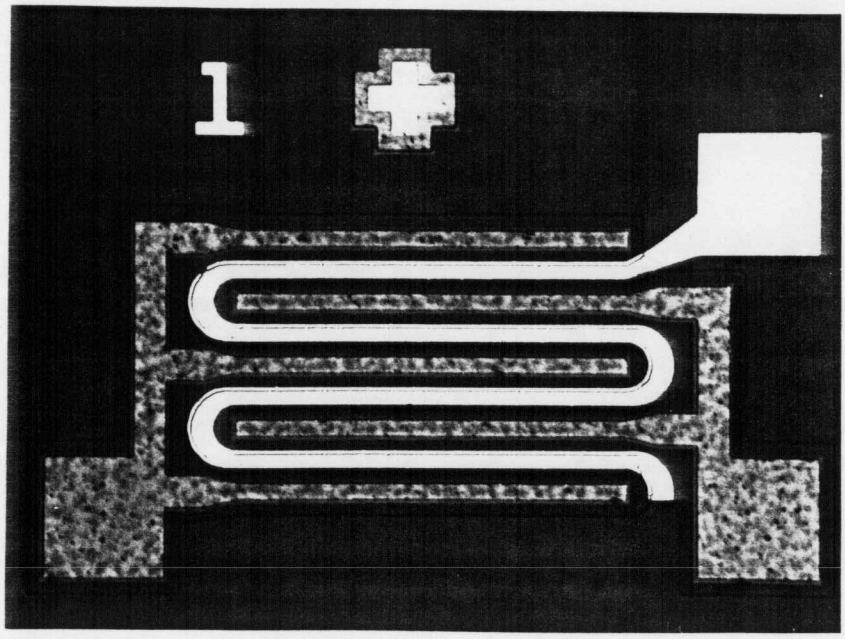



Figure 13. Optical micrograph (200×) of the interdigitated design used for the 6H-SiC p-channel MOSFET devices. The source and drain contacts are located at the lower left and right, respectively, and the gate contact is in the upper right corner. The gate length and width are 7 μm and 1 mm, respectively.

Three potential solutions were determined for this problem. The first would be to form a self-aligned gate, where the oxide does not overlap the $p^+$ source and drain. However, this would require ion implanting $Al^+$ post oxidation using the gate contact as the implant mask. As stated earlier, it is doubtful that this process could be achieved with any success in a reasonable time frame. The second method would be to replace the Al with another p-type dopant that would not degrade the electrical integrity of the oxide. However, the only likely candidate for this would be boron. Boron is typically observed to be a much deeper level p-type dopant than Al, making the ability to obtain $p^+$ material even more difficult. Although processes for obtaining $p^+$ material with B could be developed, this was beyond the scope of this research. The third method for solving the problem was to eliminate the Al from the oxide by growing a thin undoped layer of SiC on top of the $p^+$ material and letting it be consumed by the oxidation process. It was decided to pursue the latter method.

Therefore, the next batch of p-channel MOSFETs were grown just as was shown in Fig. 12(a). However, after the $p^+$ mesas were reactive ion etched, an additional epitaxial layer of undoped 6H-SiC, approximately 385 Å thick, was grown on the wafers. The Si-face wafers were then oxidized at two different temperatures. Three wafers were oxidized at 1300°C in wet $O_2$ for 11 minutes and the other four were oxidized at 1200°C in wet $O_2$ for 56 minutes, with resulting oxide thicknesses of 915 Å and 730 Å, respectively. Ideally these oxidations would entirely consume the undoped SiC, resulting in an oxide that contains essentially no Al, and the $SiO_2$/SiC interface would stop just into the Al doped material. The rest of the device fabrication for these devices was identical to that described for the previous batch. This would give a final structure identical to that shown in Fig. 12(b), except that the $SiO_2$ would not contain any Al where the gate contact overlaps the $p^+$ mesa.

The results of this second batch were unfortunately unsuccessful, although it did show some promising results. The encouraging result was that there was no detectable gate leakage current on most of the devices measured. The oxides showed very good electrical insulation to biases greater than 20 V. The C-V curves of the gate oxides were also very good, as shown in Fig. 14. This C-V curve was measured on a relatively large area gate (20 μm × 1 mm) and shows a room temperature flat band voltage and threshold voltage of +1.1 V and -4.0 V, respectively. The fixed oxide space charge was less than $5\times10^{10}$ $cm^{-2}$. The channel doping was calculated to be about $5\times10^{16}$ $cm^{-3}$, which is somewhat higher than the $2.1\times10^{16}$ $cm^{-3}$ measured by Hg probe after epitaxial growth, but this discrepancy could be due to doping variation across the wafer. These excellent quality gate oxide layers were obtained on all of the wafers that were fabricated in this batch.

While the quality of the oxide layers was very good, none of the devices worked in the manner they were intended. The I-V characteristics shown in Fig. 15 are representative of what was obtained. For a normal p-channel device, the drain current should be negligible at zero gate bias, and then should increase as the gate is biased negatively. However, Fig. 15 shows that a maximum current of 1.35 mA was obtained at zero bias and the drain current <u>decreased</u> as the gate was biased negatively. Also, no current saturation was observed.

Since the drain current decreases with negative gate bias, it is apparent that the device is acting more like a depletion-mode MOSFET, where the source, drain, and

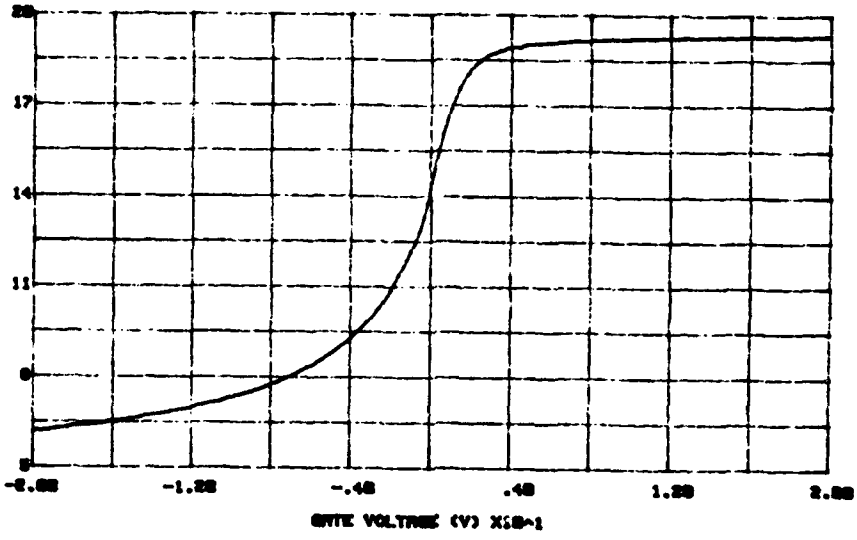


Figure 14. Capacitance-voltage curve of the gate oxide of a 6H-SiC p-channel MOSFET device. The gate length and width was 20 μm and 1 mm, respectively. With the contact pad, the gate contact area was $4.15 \times 10^{-4}$ $cm^2$.

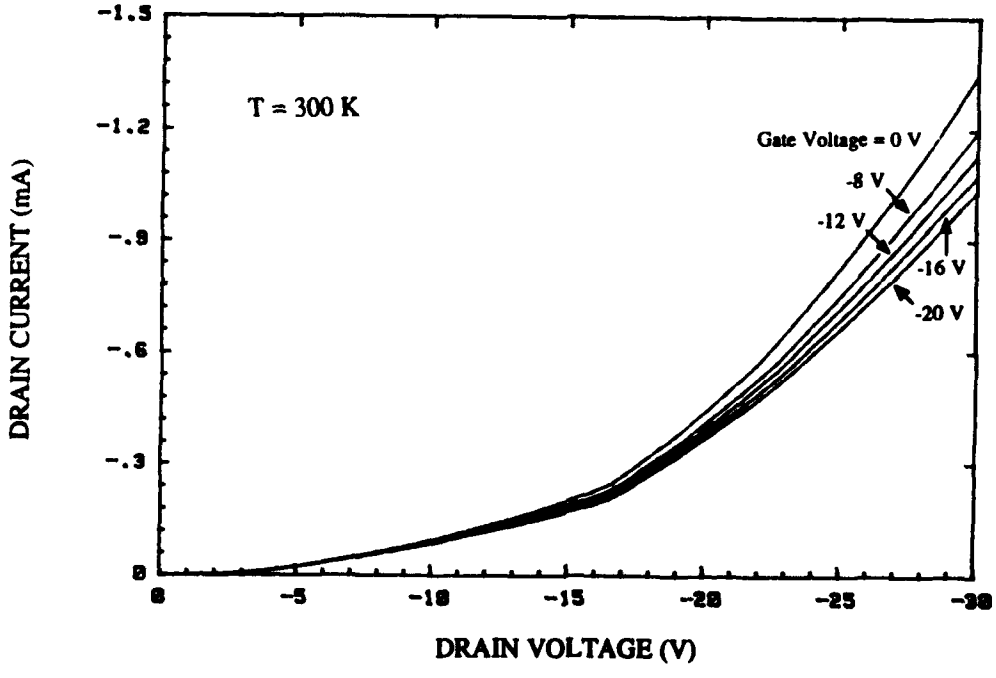



Figure 15. Drain I-V curves of a 6H-SiC p-channel MOSFET device. The gate length and width was 7 μm and 1 mm, respectively.

channel are all n-type and the channel is depleted and pinched off by applying a negative gate bias. This is what one would expect if the thin intrinsic layer that was deposited on the $p^+$ mesas was not entirely consumed during oxidation. A thin intrinsic layer from source to drain would simply act like a resistive short that was variable with gate bias. This could happen if the intrinsic epilayer was thicker than expected, or if the calculated ratio of SiC consumed to $SiO_2$ thickness grown was inaccurate. The ratio used was 0.47 which was calculated from the relative Si densities in SiC versus that in $SiO_2$. The Si density in SiC is known, but the density of Si in $SiO_2$ grown on SiC was not known, therefore the Si density in $SiO_2$ grown on Si was used for the calculation. Since there has been very little investigation of either thin epilayer growth rates or $SiC/SiO_2$ consumption ratios, it is not known which is more likely or if both factors played a role.

From the good gate oxide results that were obtained, it is apparent that p-channel MOSFETs with desirable characteristics could be fabricated with further development. This would require experimentation to more accurately calculate the $SiC/SiO_2$ consumption ratio and more accurately grow very thin layers of SiC.

### B. n-channel MOSFETs

Good results were shown in the proposal for C-face planar MOSFET wafers utilizing the same mesa-style source and drains that were used for the p-channel devices. The maximum transconductance of these devices was 1.4 mS/mm and the threshold voltage ($V_T$) was around $V_G$ = +6 V. The good results were attributed to the much lower doped p-type channel layer ($p = 2.5x10^{15}$ $cm^{-3}$) that was used.

Since reducing the Al concentration in the oxide and at the interface helped the transfer characteristics of the MOSFETs, and the C-V curves of n-type material looked almost theoretically perfect, it was decided to try eliminating Al entirely from the oxide. These devices were fabricated on the Si-face of n-type substrates and utilized ion implanted $n^+$ source and drain wells instead of the mesa-style. The major difference between this batch and previous batches of n-channel MOSFETs was that a very thin layer of undoped 6H-SiC was grown on top of the p-channel layer. The p-type layer was first grown and measured to have $p = 4.3x10^{15}$ $cm^{-3}$ and a thickness of 6 μm. Then an epitaxial layer of undoped SiC only 37 nm thick ($n = 2\text{-}8x10^{15}$ $cm^{-3}$) was grown on top. It was intended that this layer be consumed during the oxidation

and that the $SiO_2$/SiC interface stop at a point very close to the p-type material, or only a monolayer or two into it. This is similar to what was attempted for the p-channel MOSFETs, except there were no etched mesas on the wafer when the thin undoped layer was grown.

The devices were fabricated as follows. Polysilicon was first deposited and patterned on the surface of the wafers for use as a high temperature ion implant mask. The source and drain wells were then implanted at 650°C with $N^+$. The polysilicon was stripped and the wafers were then annealed at high temperature. The wafers were subsequently oxidized in wet $O_2$ at 1200°C for 49 minutes, yielding an oxide thickness of 62 nm. Assuming an oxide consumption factor of 0.47, and the loss of about 6 nm in a previous RIE step, this thickness would have brought the $SiO_2$/SiC interface to within 1 nm of the p-type material, or just into it. It is not known whether the interface had Al present. However, it can be certain that there was much less Al present in the oxide than in previous MOSFETs. The final device structure is shown in cross-section in Fig. 16. The device layout was identical to that shown for the p-channel devices, shown in Fig. 13.

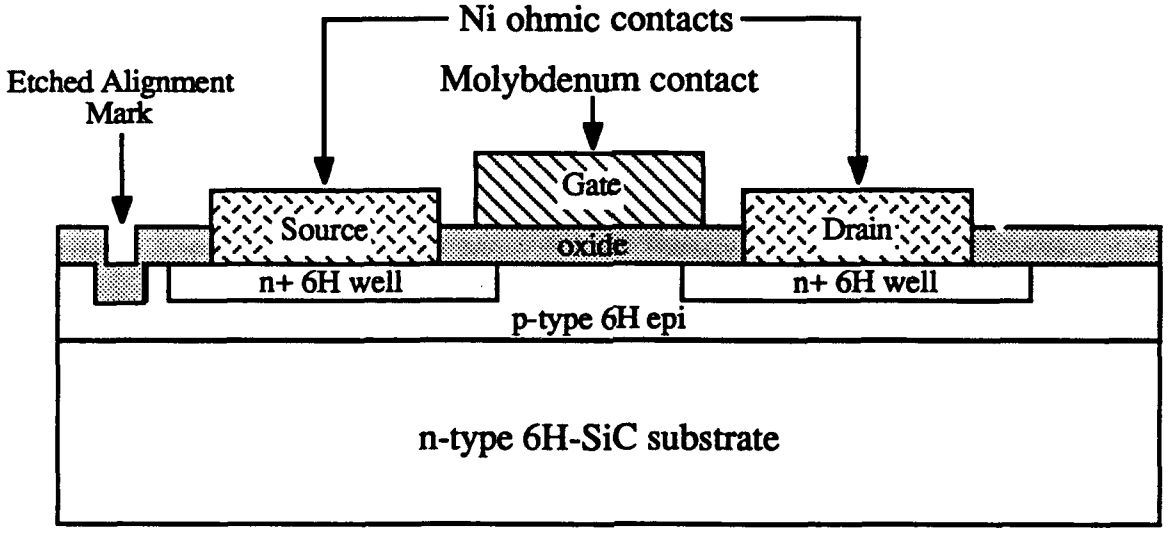



Figure 16. Cross-sectional view of the final device structure of the ion implanted 6H-SiC n-channel MOSFETs.

The room temperature I-V characteristics of these devices indicate that there was some improvement, as shown in Fig. 17. The room temperature drain current at

$V_G$ = +16 V was 18.6 mA and the transconductance at that gate voltage was 2.8 mS/mm. The threshold voltage was about 1.9 V, which is much lower than the 4-6 V reported previously. The channel mobility was measured to be about 46 $cm^2$/V-sec. The subthreshold leakage current ($V_G$ = 0 V) was 560 nA. The persistent problem of gate leakage still existed for these devices with a gate leakage of 10 μA at $V_G$ = +16 V.

The same data for this device is plotted on a different scale in Fig. 18(a) for comparison with higher temperature characteristics. When the temperature was raised to 150°C, as shown in Fig. 18(b), both the current and transconductance at $V_G$ = +16 V increased to 29 mA and 3.6 mS/mm, and the threshold voltage decreased to about -0.2 V. This trend continued up to 300°C, as shown in Fig. 18(c). At this temperature the current and transconductance at $V_G$ = +16 V were 35 mA and 3.9 mS/mm, respectively. Although the threshold voltage of the device fell to $V_G$ = -0.8 V, the drain current at $V_G$ = 0 V was only 47 μA. The channel mobility at 300°C decreased to about 43.5 $cm^2$/V-sec.

The major improvement in room temperature threshold voltage, and the threshold voltage as a function of temperature, is depicted graphically in Fig. 19. It is clear that much improvement in stabilizing the threshold voltage, and thus the transfer characteristics, has been made in the last two years, with a significant portion of the improvement attributable to this ARO funded contract. The improvement is due to the reduction of fast interface states at $SiC/SiO_2$ interface by improving the oxidation conditions and by reducing the amount of Al at the interface, as discussed previously.

While these devices showed the best I-V characteristics of any SiC MOSFETs we have seen to date, they still have room for improvement. The gate leakage problem is the foremost concern. While the gates generally start out with no measurable leakage, contact annealing seems to either cause the damage or simply allows measurement of pre-existing problems (non-annealed contacts allow very little current to flow). Another researcher, Dr. Dale Brown of GE-CRD, has not had this problem.[3] After discussion with him, we feel that the difference is probably in the annealing system. He uses a standard furnace anneal, whereas we use an RTA. Further research into the anneal is required. The other problem observed with this batch was a premature failure of the $SiO_2$ gate at high temperature. Many of the

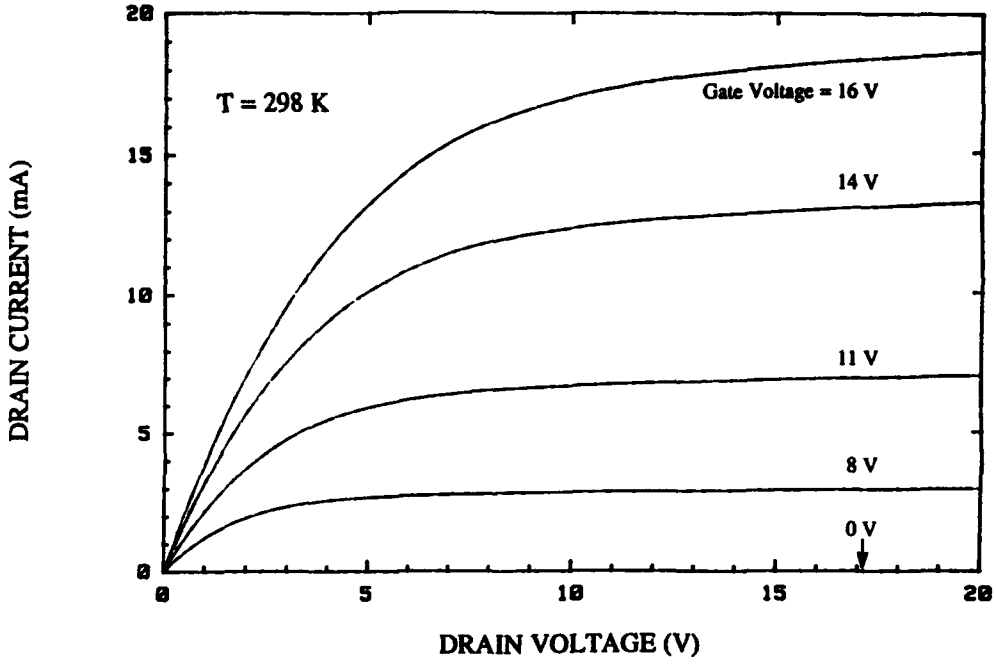



Figure 17. Room temperature drain current-voltage characteristics for an n-channel inversion-mode 6H-SiC MOSFET with a thin undoped layer oxide. The p-channel doping was $p = 4x10^{15}$ $cm^{-3}$. The gate oxide was grown on the Si-face by wet oxidation at 1200°C for 49 mins. The gate length and width were 7 μm and 1 mm, respectively, and the gate oxide was 62 nm thick.

gates would breakdown under bias between 300 and 350°C. The reason for this breakdown phenomenon is unclear at present, but this phenomenon has also been recently observed by Dr. Brown.

## VII. Conclusions

Initial testing indicates that the rectifiers developed under this program will meet the requirements of the jet engine ignitor. However, mass production of high reliability parts will require more packaging development and testing. Also, the mechanism which limits the amount of power that the devices can tolerate in avalanche should be investigated.

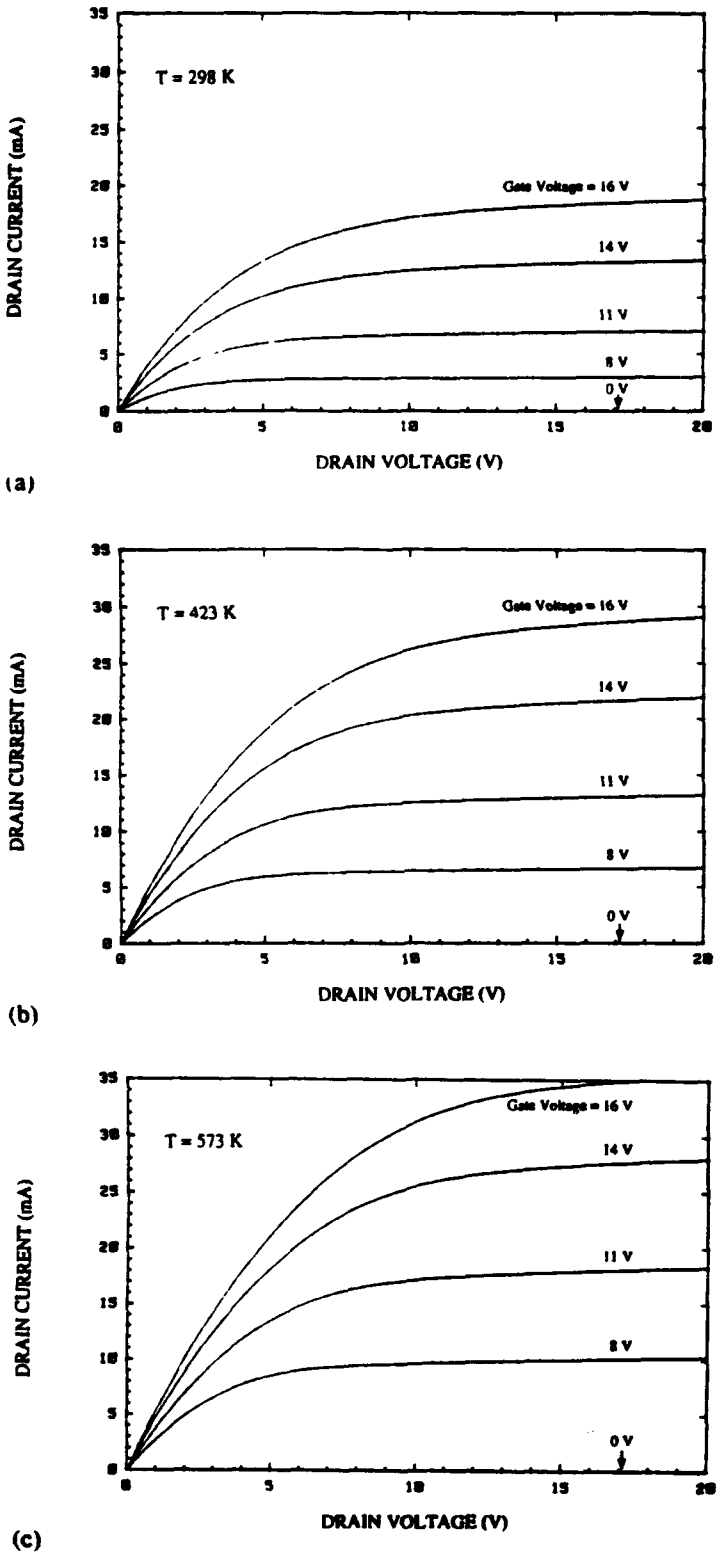



Figure 18. Drain current-voltage characteristics for the n-channel inversion-mode 6H-SiC MOSFET shown in Fig. 12 at (a) 25°C, (b) 150°C, and (c) 300°C.

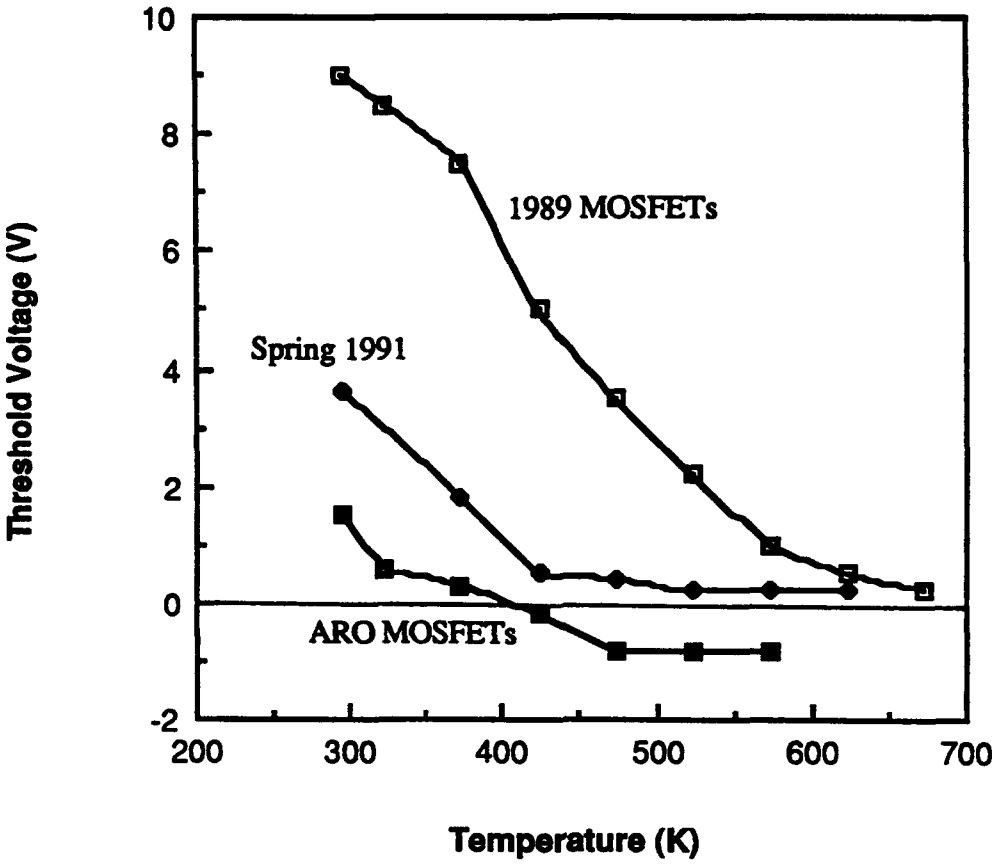



Figure 19. Stabilization of threshold voltage as a function of temperature for n-channel inversion-mode 6H-SiC MOSFETs over the last two years.

Although no operable p-channel 6H-SiC MOSFETs were achieved, significant progress was made in understanding the mechanisms that affect their performance. In particular, high Al-doping in the $p^+$ source and drain mesas was found to cause excessive leakage current through the thermally grown oxides. A method was developed which should circumvent this problem but the limited scope and time of this contract did not allow this process to be successfully demonstrated. However, this method was applied with success to n-channel MOSFETs which are also negatively affected by Al in the oxide. These devices showed improved transfer characteristics over those previously demonstrated in SiC. Improvement of the $SiO_2$/SiC interface is a subject which requires much more research.

## VIII. Publications and Technical Reports

1. J.A. Edmond, J.W. Palmour and C.H. Carter, Jr., "Junction Devices in 6H-SiC", in Proceedings of the 1991 International Semiconductor Device Research Symposium, (Charlottesville, VA; December 1991) pp.487-490.

2. J.W. Palmour, H.S. Kong and C.H. Carter, Jr., "Field-Effect Transistors in 6H-Silicon Carbide", in Proceedings of the 1991 International Semiconductor Device Research Symposium, (Charlottesville, VA; December 1991) pp.487-490.

3. J.W. Palmour, J.A. Edmond, H.S. Kong and C.H. Carter, Jr., "Applications for 6H-Silicon Carbide Devices", presented at the Fourth International Conference on Amorphous and Crystalline Silicon Carbide and Other IV-IV Compounds, Oct. 10-11, 1991, Santa Clara, CA. To be published by Springer-Verlag.

## IX. Participating Scientific Personnel

Dr. Calvin H. Carter, Jr. - Director of Technology
Dr. John A. Edmond - Senior Scientist
Dr. John W. Palmour - Senior Scientist

No advanced degrees were earned due to employment on this project.

## X. Report of Inventions

John W. Palmour, "Method for Obtaining High Quality $SiO_2$ Passivation on Silicon Carbide Structures", Cree Invention Disclosure #028.

## XI. Bibliography


1. S.M. Tang, W.B. Berry, R. Kwor, M.V. Zeller, and L.G. Matus, *J. Electrochem. Soc.*, **137**, 221 (1990).
2. D.M. Brown, M. Ghezzo, J. Kretchmer, E. Downey, T. Gorczyca, R. Saia, J. Edmond, J. Palmour, C.H. Carter, Jr., G. Gati, S. Dasgupta, J. Pimbley, and P. Chow, to be published in the Proceedings of GOMAC-91, presented Nov.4-7, 1991 in Orlando, Florida.
3. D.M. Brown, private communication, General Electric - Corporate Research and Development, Schenectady, NY.